AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of performing bus inversion on first bits to be transmitted on a bidirectional bus from a first device to a second device, said method comprising the steps of:

~~determining whether the first device will drive output data during a next drive cycle; and~~

~~if it is determined that the first device will drive output data during the next drive cycle:~~

capturing a state of previously transmitted bits on the bidirectional bus with a first clocked register according to a clock signal,

capturing a state of an inversion bit associated with the previously transmitted bits with a second clocked register according to the clock signal, and

determining from the captured state of the previously transmitted bits whether the first bits should be inverted.

2. (Original) The method of claim 1 further comprising the step of inverting the first bits if it is determined that the first bits should be inverted.

3. (Original) The method of claim 2 further comprising the steps of:

outputting the inverted first bits on the bus; and

outputting the inversion bit with a value indicating that the first bits have been inverted.

4. (Original) The method of claim 1 further comprising the steps of:

outputting the first bits on the bus; and

outputting the inversion bit with a value indicating that the first bits have not been inverted.

5. (Original) The method of claim 1, wherein said determining step comprises:

obtaining a number of first bits that match the previously transmitted bits;

determining whether the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits; and

setting the inversion bit to a value indicating that the first bits should not be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits.

6. (Original) The method of claim 5 further comprising the steps of:

determining whether the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits; and

setting the inversion bit to the captured state of the inversion bit if it is determined that the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits.

7. (Original) The method of claim 6, wherein the number of first bits is an even number.

8. (Original) The method of claim 6 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than or equal to one half the number of first bits.

9. (Original) The method of claim 5 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits.

10. (Original) The method of claim 9, wherein the number of first bits is an odd number.

11. (Original) The method of claim 1, wherein said capturing steps are performed only when the first bits are available for transfer over the bus.

12. (Original) The method of claim 1, wherein said capturing steps are performed for every transfer on the bus.

13. (Original) The method of claim 1, wherein said determining step is based on reducing a number of transitions of the first bits and the inversion bit.

14. (Original) The method of claim 1, wherein said determining step is based on reducing the number of first bits having a predetermined logical state.

15. (Original) The method of claim 14, wherein the predetermined logical state is a logical one.

16. (Original) The method of claim 14, wherein the predetermined logical state is a logical zero.

17. (Currently Amended) A method of outputting first bits on a bidirectional bus from a first device to a second device, said method comprising the acts of:

~~determining whether the first device will drive output data during a next drive cycle; and~~

~~if it is determined that the first device will drive output data during the next drive cycle:~~

determining from a previous state of the bidirectional bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted;

if it is determined that first bits should be inverted,

outputting inverted first bits on the bidirectional bus, and

outputting on a separate line, with a clocked register according to a clock signal, the inversion bit with a value indicating that the first bits have been inverted; and

if it is determined that first bits should not be inverted,

outputting the first bits on the bidirectional bus, and

outputting on [[a]] the separate line, with the clocked register according to the clock signal, the inversion bit with a value indicating that the first bits have not been inverted.

18. (Original) The method of claim 17, wherein said determining step comprises:

obtaining a number of first bits that match a state of previously transmitted bits;

determining whether the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits; and

setting the inversion bit to a value indicating that the first bits should not be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits.

19. (Original) The method of claim 18 further comprising the steps of:

determining whether the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits; and

setting the inversion bit to a previous state of the inversion bit if it is determined that the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits.

20. (Original) The method of claim 19 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than or equal to one half the number of first bits.

21. (Original) The method of claim 18 further comprising the step of setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits.

22. (Original) The method of claim 17, wherein said determining step is based on reducing a number of transitions of the first bits and the inversion bit.

23. (Original) The method of claim 17, wherein said determining step is based on reducing the number of first bits having a predetermined logical state.

24. (Original) The method of claim 23, wherein the predetermined logical state is a logical one.

25. (Original) The method of claim 23, wherein the predetermined logical state is a logical zero.

26. (Currently Amended) A system comprising:

a first device; and

a second device connected to said first device by a first bidirectional bus and an associated inversion bit line, said first device being configured for transmitting first bits over the first bidirectional bus to the second device by:

~~determining whether the first device will drive output data during a next drive cycle; and~~

~~if it is determined that the first device will drive output data during the next drive cycle:~~

capturing a state of previously transmitted bits on the first bidirectional bus with a first clocked register according to a clock signal,

capturing a state of an inversion bit on the inversion bit line with a second clocked register according to the clock signal, and

determining from the captured state of the previously transmitted bits whether the first bits should be inverted.

27. (Previously Presented) The system of claim 26, wherein said first device is further configured for inverting the first bits if it is determined that the first bits should be inverted.

28. (Previously Presented) The system of claim 27, wherein said first device is further configured for:

outputting the inverted first bits on the first bus, and

outputting the inversion bit on the inversion bit line with a value indicating that the first bits have been inverted.

29. (Previously Presented) The system of claim 26, wherein said first device is further configured for:

outputting the first bits on the first bus, and

outputting the inversion bit with a value indicating that the first bits have not been inverted.

30. (Previously Presented) The system of claim 26, wherein said first device is further configured for:

determining whether the first bits should be inverted by obtaining a number of first bits that match the previously transmitted bits,

determining whether the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits, and

setting the inversion bit to a value indicating that the first bits should not be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is greater than one half the number of first bits.

31. (Previously Presented) The system of claim 30, wherein if said first device determines that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits, said first device is further configured for:

determining whether the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits, and

setting the inversion bit to the captured state of the inversion bit if it is determined that the obtained number of first bits that match the previously transmitted bits is equal to one half the number of first bits.

32. (Previously Presented) The system of claim 31, wherein said first device is further configured for:

setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than or equal to one half the number of first bits.

33. (Previously Presented) The system of claim 30, wherein said first device is further configured for:

setting the inversion bit to a value indicating that the first bits should be inverted if it is determined that the obtained number of first bits that match the previously transmitted bits is not greater than one half the number of first bits.

34. (Previously Presented) The system of claim 26, wherein said first device is further configured for:

capturing the states of the previously transmitted bits and inversion bit only when the first bits are available for transfer over the first bus.

35. (Previously Presented) The system of claim 26, wherein said first device is further configured for:

capturing the states of the previously transmitted bits and inversion bit for every transfer on the first bus.

36. (Previously Presented) The system of claim 26, wherein said first device is further configured for:

determining whether to invert the first bits based on reducing a number of transitions of the first bits and the inversion bit.

37. (Previously Presented) The system of claim 26, wherein said first device is further configured for:

determining whether to invert the first bits based on reducing the number of first bits having a predetermined logical state.

38. (Previously Presented) The system of claim 26, wherein the first bus comprises an address bus.

39. (Previously Presented) The system of claim 26, wherein the first bus comprises a portion of an address bus.

40. (Previously Presented) The system of claim 26, wherein the first bus comprises a command bus.

41. (Previously Presented) The system of claim 26, wherein the first bus comprises a data bus.

42. (Previously Presented) The system of claim 26, wherein the first bus comprises a portion of a data bus.

43. (Original) The system of claim 26, wherein a number of first bits comprises four bits.

44. (Original) The system of claim 26, wherein a number of first bits comprises eight bits.

45. (Original) The system of claim 26, wherein a number of first bits comprises nine bits.

46. (Original) The system of claim 26, wherein a number of first bits comprises sixteen bits.

47. (Original) The system of claim 26, wherein a number of first bits comprises thirty-two bits.

48. (Currently Amended) A system comprising:

a first device; and

a second device connected to the first device by a plurality of bidirectional buses, at least a first bidirectional bus of said plurality of bidirectional buses being associated with a first inversion bit line, said first device being configured for transmitting first bits over the first bidirectional bus by:

~~determining whether the first device will drive output data during a next drive cycle; and~~

~~if it is determined that the first device will drive output data during the next drive cycle:~~

determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted,

wherein:

if it is determined that first bits should be inverted, outputting inverted first bits on the first bidirectional bus and outputting the inversion bit, with a clocked register according to a clock signal, with a value indicating that the first bits have been inverted, and

if it is determined that first bits should not be inverted, outputting the first bits on the first bidirectional bus and outputting the inversion bit, with the clocked register according to the clock signal, with a value indicating that the first bits have not been inverted.

49. (Previously Presented) The system of claim 48, wherein said first device is further configured for determining whether to invert the first bits based on reducing a number of transitions of the first bits and the inversion bit.

50. (Previously Presented) The system of claim 48, wherein said first device is further configured for determining whether to invert the first bits based on reducing the number of first bits having a predetermined logical state.

51. (Previously Presented) The system of claim 48, wherein the first bus comprises an address bus.

52. (Previously Presented) The system of claim 48, wherein the first bus comprises a portion of an address bus.

53. (Previously Presented) The system of claim 48, wherein the first bus comprises a command bus.

54. (Previously Presented) The system of claim 48, wherein the first bus comprises a data bus.

55. (Previously Presented) The system of claim 48, wherein the first bus comprises a portion of a data bus.

56. (Original) The system of claim 48, wherein a number of first bits comprises four bits.

57. (Original) The system of claim 48, wherein a number of first bits comprises eight bits.

58. (Original) The system of claim 48, wherein a number of first bits comprises nine bits.

59. (Original) The system of claim 48, wherein a number of first bits comprises sixteen bits.

60. (Original) The system of claim 48, wherein a number of first bits comprises thirty-two bits.

61. (Previously Presented) The system of claim 48, wherein:

a second bus of said plurality of buses being coupled to a respective second inversion bit line and said first device being further configured for:

transmitting second bits over the second bus by determining from a previous state of the second bus and a previous state of a second inversion bit on the second inversion bit line whether the second bits should be inverted,

if it is determined that second bits should be inverted, outputting inverted second bits on the second bus and outputting the second inversion bit with a value indicating that the second bits have been inverted, and

if it is determined that second bits should not be inverted, outputting the second bits on the second bus and outputting the second inversion bit with a value indicating that the second bits have not been inverted.

62. (Currently Amended) A system comprising:

first, second, and third devices connected to each other by a first bidirectional bus and an associated inversion bit line, said first device being configured for transmitting first bits over the first bidirectional bus to one of the second and third device by:

~~determining whether the first device will drive output data during a next drive cycle; and~~

~~if it is determined that the first device will drive output data during the next drive cycle:~~

capturing a state of previously transmitted bits on the first bidirectional bus with a first clocked register according to a clock signal,

capturing a state of an inversion bit on the inversion bit line with a second clocked register according to the clock signal, and

determining from the captured state of the previously transmitted bits whether the first bits should be inverted.

63. (Currently Amended) A system comprising:

~~means for determining whether the first device will drive output data during a next drive cycle;~~

means for capturing a state of previously transmitted bits on a bidirectional bus with a first clocked register according to a clock signal;

means for capturing a state of an inversion bit associated with the previously transmitted bits with a second clocked register according to the clock signal;

means for determining from the captured state of the previously transmitted bits whether the first bits should be inverted;

means for transmitting inverted first bits on the bidirectional bus and an inversion bit, with a second clocked register according to the clock signal, having a value indicating that the first bits have been inverted if it has been determined from the captured state of the previously transmitted bits that the first bits should be inverted; and

means for transmitting the first bits on the bidirectional bus and an inversion bit, with a second clocked register according to the clock signal, having a value indicating that the first bits have not been inverted if it has been determined from the captured state of the bits that the first bits should not be inverted.

64. (Previously Presented) A system comprising:

a bidirectional bus;

an inversion bit line;

a first device being configured for transmitting first bits over the bidirectional bus, the first device comprising:

~~a first determining circuit for determining whether the first device will drive output data during a next drive cycle,~~

a first capture circuit for capturing a state of previously transmitted bits on the bidirectional bus with a first clocked register according to a clock signal,

a second capture circuit for capturing a state of an inversion bit on the inversion bit line with a second clocked register according to the clock signal, and

a second determining circuit for determining from the captured state of the previously transmitted bits whether the first bits should be inverted; and

a second device connected to the first device by the bidirectional bus and the inversion bit line.